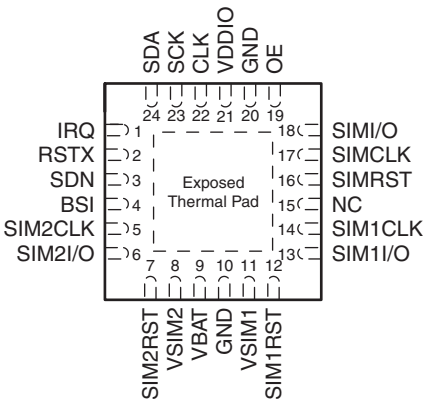
DUAL-SUPPLY 2:1 SIM CARD MULTIPLEXER/TRANSLATOR WITH AUTOMATIC DETECTION AND SLOT DEDICATED DUAL LDO

Check for Samples: TXS02326

FEATURES

- **Level Translator**
  - **V_I/O Range of 1.7 V to 3.3 V**
- **Low-Dropout (LDO) Regulator**
  - **50-mA LDO Regulator With Enable**
  - **1.8-V or 2.95-V Selectable Output Voltage**
  - **2.3-V to 5.5-V Input Voltage Range**
  - **Very Low Dropout: 100 mV (Max) at 50 mA**
- **Control and Communication Through I^2C Interface With Baseband Processor**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-B)**
  - **1000-V Charged-Device Model (C101)**
- **Package**
  - **24-Pin QFN (4 mm x 4 mm)**

RGE PACKAGE
(TOP VIEW)



Note: The Exposed Thermal Pad must be connect to Ground.

DESCRIPTION/ORDERING INFORMATION

The TXS02326 is a complete dual-supply standby Smart Identity Module (SIM) card solution for interfacing wireless baseband processors with two individual SIM subscriber cards to store data for mobile handset applications. It is a custom device which is used to extend a single SIM/UICC interface to be able to support two SIMs/UICCs.

The device complies with ISO/IEC Smart-Card Interface requirements as well as GSM and 3G mobile standards. It includes a high-speed level translator capable of supporting Class-B (2.95 V) and Class-C (1.8 V) interfaces, two low-dropout (LDO) voltage regulators that have output voltages that are selectable between 2.95-V Class-B and 1.8-V Class-C interfaces, an integrated "fast-mode" 400 kb/s "slave" I2C control register interface for configuration purposes, a 32-kHz clock input for internal timing generation, a shutdown input and a comparator input detecting battery pack removal to safely power-down the two SIM cards, each equipped with two programmable debounce counter (i.e. BSI input and SDN input) circuit realized by an 8 bit counter.

The voltage-level translator has two supply voltage pins. V_I/O sets the reference for the baseband interface and can be operated from 1.7 V to 3.3 V. VSIM1 and VSIM2 are programmed to either 1.8 V or 2.95 V, each supplied by an independent internal LDO regulator. The integrated LDO accepts input battery voltages from 2.3 V to 5.5 V and outputs up to 50 mA to the B-side circuitry and external Class-B or Class-C SIM card.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGE (Pin 1, Quadrant 2)	Tape and reel	TXS02326RGER	YJ326
	QFN – RGE (Pin 1, Quadrant 1)		TXS02326MRGER	YJ326

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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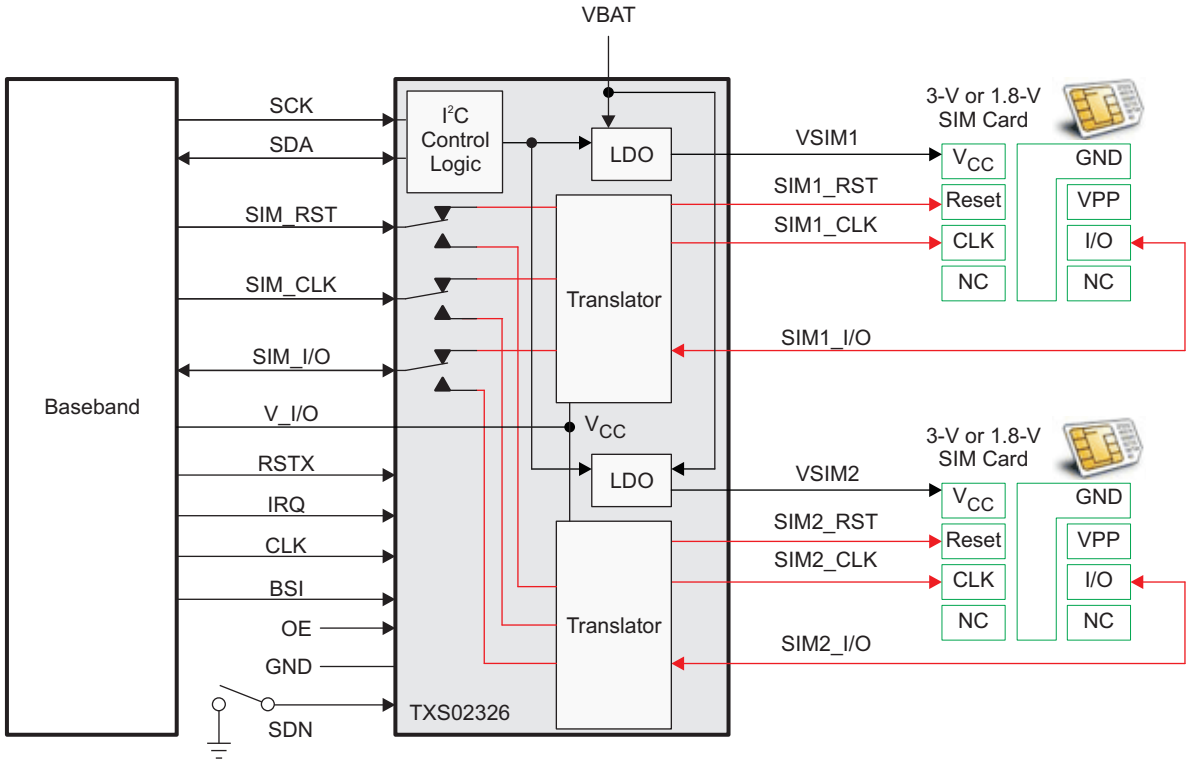


Figure 1. Interfacing With SIM Card

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TERMINAL FUNCTIONS

NO.	NAME	TYPE(1)	POWER DOMAIN	DESCRIPTION
1	IRQ	I/O	VDDIO	Interrupt to baseband. This signal is used to set the I2C address.
2	RSTX	I	VDDIO	Active-low reset input from baseband
3	SDN	I	VDDIO	Power down SIM2; for example, from switch
4	BSI	I	VDDIO	Analog signal from battery. This input accepts input voltages up to 3 V.
5	SIM2CLK	O	VSIM2	SIM2 clock
6	SIM2I/O	I/O	VSIM2	SIM2 data
7	SIM2RST	O	VSIM2	SIM2 reset
8	VSIM2	O	VSIM2	1.8 V/2.95 V supply voltage to SIM2
9	VBAT	P	VBAT	Battery power supply
10	GND	G		Ground
11	VSIM1	O	VSIM1	1.8 V/2.95 V supply voltage to SIM1
12	SIM1RST	O	VSIM1	SIM1 reset
13	SIM1I/O	I/O	VSIM1	SIM1 data
14	SIM1CLK	O	VSIM1	SIM1 clock
15	NC			No connect
16	SIMRST	I	VDDIO	UICC/SIM reset from baseband
17	SIMCLK	I	VDDIO	UICC/SIM clock
18	SIMI/O	I/O	VDDIO	UICC/SIM data
19	OE	I	VDDIO	UICC/SIM data direction from baseband
20	GND	G		
21	VDDI/O	P	VDDIO	1.8-V power supply for device operation and I/O buffers toward baseband
22	CLK	I	VDDIO	32-kHz clock
23	SCK	I	VDDIO	I^2C clock
24	SDA	I/O	VDDIO	I^2C data

(1) G = Ground, I = Input, O = Output, P = Power

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Table 1. Register Overview

REGISTER BITS								COMMAND BYTE (HEX)	REGISTER	READ OR WRITE	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	1	0	0	0	1	00h	Device hardware revision information	R	0001 0001
0	0	0	0	0	0	0	0	01h	Software revision information	R	0000 0000
SIM2 Interface Status		SIM1 Interface Status		Battery Removal Interrupt Status	Battery Status	SDN Interrupt Status	SDN Status	04h	Status Register	R	0000 0000
SIM2 Interface Status		SIM2 Voltage Select	SIM2 LDO Enable/ Disable	SIM1 Interface Status		SIM1 Voltage Select	SIM1 LDO Enable/ Disable	08h	SIM Interface Control Register	R/W	0000 0000
BSI Debounce Counter Value								0Ah	BSI Input Debounce Counter	R/W	0000 0100
SDN Debounce Counter Value								0Bh	SDN Input Debounce Counter	R/W	0000 0100
Reserved / Not Supported								0Ch	Reserved	R/W	0000 0000
Clock Source Select	Clock Control (Reserved)							0Dh	External Clock Control	R/W	0000 0000
SDN Detection Behavior control	SDN Level Detection Select	SDN Interrupt Enable/ Disable	BSI Detection Behavior Control	BSI Level Detection Select	Battery Removal Interrupt Enable/ Disable	OE Direction Control	OE Control Select	0Eh	Device Control Register	R/W	0000 0000
								10h-14h	Device-specific testing	R/W	xxxx xxxx
Reserved						SDN Pull-down Enable/ Disable	SDN Pull-up Enable/ Disable	15h	General purpose	R/W	0000 0000

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Table 2. Device Hardware Revision Register (00h)

Device HW Driver Register	Bits(s)	Type (R/W)	Description
HW identification	7:0	R	This register contains the manufacturer and device ID(1) (value to be specified by the manufacturer)

(1) The manufacturer ID part of this data shall remain unchanged when the HW revision ID is updated. The manufacturer ID shall uniquely identify the manufacturer. The manufacturer ID is encoded on the MSB nibble.

Table 3. Device Software Revision Register (01h)

Device SW Driver Register	Bits(s)	Type (R/W)	Description
SW Driver Version	7:0	R	This register contains information about the SW driver required for this device. This information shall only be updated when changes to the device requires SW modifications. Initial register value is 00h

Table 4. Status Register (04h)

Status Register	Bits(s)	Type (R/W)	Description
SDN Status(1)	0	R	SDN signal state captured after debounce counter has expired '0' SDN signal at GND '1' SDN signal at V_I/O level
SDN Interrupt(1)	1	R	SDN interrupt status '0' No interrupt '1' Interrupt occurred, (the read operation will automatically clear this bit)
Battery Status	2	R	'0' Battery present '1' Battery not present, i.e. debounce counter expired
Battery Removal Interrupt	3	R	Battery removal interrupt status '0' No interrupt '1' Interrupt occurred, (the read operation will automatically clear this bit)
SIM1 Interface Status [1:0]	5:4(2)	R	Status of SIM1 interface '00' Powered down with pull-downs activated '01' Isolated with pull-downs deactivated '10' Powered with pull downs activated '11' Active with pull downs deactivated
SIM2 Interface Status [1:0]	7:6(2)	R	Status of SIM2 interface '00' Powered down with pull-downs activated '01' Isolated with pull-downs deactivated '10' Powered with pull downs activated '11' Active with pull downs deactivated

(1) The SDN status bit indicates the state of the SDN signal at the input when the debounce counter expired, i.e. when the SDN interrupt bit is set.
(2) The content of bits 5:4 and 7:6 reflects the value written to the state bits in the SIM Interface control register 3:2 and 7:6 respectively and the setting of the regulator bits in the SIM interface control register 0 and 4 respectively.

Table 5. State and Status Bit Mapping

SIM interface control register state bits 3:2 and 7:6	SIM interface control register regulator control bits 0 and 4	SIM status register bits 5:4 and 7:6	Comment
'00' Powered down state with pull-downs activated	'0' Regulator is off, regulator output is pulled down	'00' Powered down with pulldowns activated	
'00' Powered down state with pull-downs activated	'1' Regulator is powered on, regulator output pull-down is released	'10' Powered with pull-downs activated	
01' Isolated state with pulldowns deactivated	'0' Regulator is off, regulator output is pulled down	'00' Powered down with pulldowns activated	The interface can only be in isolated state when the interface is powered

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Table 5. State and Status Bit Mapping (continued)

SIM interface control register state bits 3:2 and 7:6	SIM interface control register regulator control bits 0 and 4	SIM status register bits 5:4 and 7:6	Comment
'01' Isolated state with pulldowns deactivated	'1' Regulator is powered on, regulator output pull-down is released	'01' Isolated with pull-downs deactivated	
'10' Not allowed	'0' Regulator is off, regulator output is pulled down	'00' Powered down with pulldowns activated	This combination shall not be used. If used the status bit coding is as specified
10' Not allowed	'1' Regulator is powered on, regulator output pull-down is released	'10' Powered with pull downs activated	This combination shall not be used. If used the status bit coding is as specified
'11' Active state with pull-downs deactivated	'0' Regulator is off, regulator output is pulled down	'00' Powered down with pulldowns activated	The interface can only be active if it is powered
11' Active state with pull-downs deactivated	'1' Regulator is powered on, regulator output pull-down is released	'11' Active with pull-downs deactivated	

Table 6. SIM Interface Control Register (08h)(1)(2)

Status Register	Bit(s)	Type (R/W)	Description
SIM1 Regulator Control	0	R/W	'0' Regulator is off, regulator output is pulled down '1' Regulator is powered on, regulator output pull-down is released
SIM1 Regulator Voltage Selection	1	R/W	'0' 1.8 V '1' 2.95 V
SIM1 Interface State [1:0]	3:2	R/W	Status of SIM1 interface '00' Powered down state with pull-downs activated '01' Isolated state with pull-downs deactivated '10' Not allowed '11' Active state with pull downs deactivated
SIM2 Regulator Control	4	R/W	'0' Regulator is off, regulator output is pulled down '1' Regulator is powered on, regulator output pull-down is released
SIM2 Regulator Voltage Selection	5	R/W	'0' 1.8 V '1' 2.95 V
SIM2 Interface State [1:0]	7:6	R/W	Status of SIM2 interface '00' Powered down state with pull-downs activated '01' Isolated state with pull-downs deactivated '10' Not allowed '11' Active state with pull downs deactivated

(1) Reset value: 00h
(2) The state '10', on bits 3:2 and 7:6, is not prevented by HW but shall never be set by SW. State '10' means that the interface is powered with the pull-downs active, this state correspond to state '00' with the regulator being switched on. Setting the state to '10' does not have any impact on the corresponding regulator bit setting. The regulator control bits do not impact the state bits in this register. The regulator control bits however do impact the status bits in the status register.

Table 7. Battery Presence Detection Debounce Counter (0Ah)(1)(2)

BSI Debounce Counter	Bits(s)	Type (R/W)	Description
Debounce Counter Value [7:0]	7:0	R/W	This register contains the BSI input debounce counter value. The value 00h means that the counter is not used, i.e. no debounce.

(1) Reset value: 04h
(2) Updating the register causes the counter to restart with the new value if the counter is counting when the register is updated. The new value shall take affect no later than one clock cycle (32 KHz) after the register has been updated.

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Table 8. SDN Input Debounce Counter (0Bh)(1)(2)

SDN Debounce Counter	Bits(s)	Type (R/W)	Description
Debounce Counter Value [7:0]	7:0	R/W	This register contains the SDN input debounce counter value. The value 00h means that the counter is not used, i.e. no debounce.

(1) Reset value: 04h
(2) Updating the register causes the counter to restart with the new value if the counter is counting when the register is updated. The new value shall take affect no later than one clock cycle (32 KHz) after the register has been updated.

Table 9. External Clock Control (0Dh)(1)

Clock Control Register	Bits(s)	Type (R/W)	Description
Clock Control	6:0	R/W	Reserved
Clock Source Select	7	R/W	'0' Internal clock source used '1' External clock source CLK (supplied on pin 22 used)

(1) Reset value: 00h

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Table 10. Device Control Register (0Eh)(1)

Clock Control Register	Bits(s)	Type (R/W)	Description
OE Control	0	R/W	'0' OE is not used to control the data direction on the selected SIM I/O and the base band I/O '1' OE controls the data direction, see below
OE Direction Control	1	R/W	'0' OE input = '0' data direction Base band -> SIM OE input = '1' data direction SIM -> base band '1' OE input = '0' data direction SIM -> base band OE input = '1' data direction Base band -> SIM
Battery Removal Interrupt	2	R/W	'0' Battery removal interrupt disabled '1' Battery removal detected causes interrupt on IRQ (interrupt sets b3 in the status register)
BSI Level Detection	3	R/W	BSI detection level '0' 1.2V '1' 1.65V
BSI Detection Control	4	R/W	BSI detection behavior '0' Battery not present causes automatic power down of both SIM interfaces '1' Battery not present doesn't cause automatic power down
SDN Detection Interrupt	5	R/W	'0' SDN detection interrupt disabled '1' SDN detected causes interrupt on IRQ (interrupt sets b1 in the status register)
SDN Detection Level	6	R/W	SDN input active level '0' SDN is active low i.e. automatic shutdown occurs when debounced SDN is low. '1' SDN is active high i.e. automatic shutdown occurs when debounced SDN is high
SDN Detection Control	7	R/W	Disable automatic power down upon SDN detection '0' SDN detection causes automatic power down of SIM2 interface '1' SDN detection doesn't cause automatic power down of SIM2 interface

(1) Reset value: 00h

Table 11. General Purpose Register (15h)(1)

Function	Bit(s)	Type (R/W)	Description
SDN pull-up control	0	R/W	'0' SDN input pull-up enabled '1' SDN input pull-up disabled
SDN pull-down control	1	R/W	'0' SDN pull-down disabled '1' SDN pull-down enabled
RFU	7:2	R/W	

(1) The RFU bits shall allow for the write operation to complete but shall read as '0'. The SW should write '0' into these locations, reset value.

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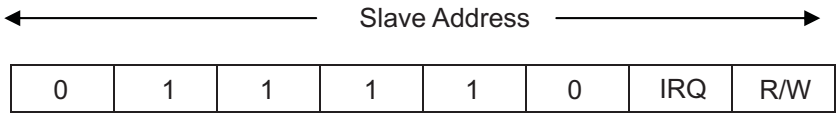
BASIC DEVICE OPERATION

The TXS02326 is controlled through a standard I^2C interface reference to VDDIO. It is connected between the two SIM card slots and the SIM/UICC interface of the baseband. The device uses VBAT and VDDI/O as supply voltages. The supply voltage for each SIM card is generated by an on-chip low drop out regulator. The interface between the baseband and the TXS02326 is reference to VDDIO while the interface between the TXS02326 and the SIM card is referenced to the LDO output of either VSIM1 or VSIM2 depending on which slot is being selected. The VDDIO on the baseband side normally does not exceed 1.8V, thus voltage level shifting is needed to support a 3V SIM/UICC interface (Class B).

The TXS02326 has two basic states, the reset and operation state. The baseband utilizes information in the status registers to determine how to manipulate the control registers to properly switch between two SIM cards. These fundamental sequences are outlined below and are to help the user to successfully incorporate this device into the system.

DEVICE ADDRESS

The address of the device is shown below:



Address Reference

IRQ@ Reset	R/W	Slave Address
0	0 (W)	120 (decimal), 78(h)
0	1 (R)	121 (decimal), 79(h)
1	0 (W)	122 (decimal), 7A(h)
1	1 (R)	123 (decimal), 7B(h)

RESET STATE

In the reset state the device settings are brought back to their default values and any SIM card that has been active is deactivated. After reset, neither of the UICC/SIM interfaces is selected. The active pull-downs at the UICC/SIM interface are automatically activated. To ensure the system powers up in an operational state, device uses an internal 32 KHz clock for internal timing generation. After power up, the system has the option to continue to utilize the internal clock or select an external clock source. This clock source is selectable by the Clock Source Select I^2C register bit.

- Power up the TXS02326 by asserting VBAT to enter the operation state
- I^2C Interface becomes active with the VDD_I/O supply

RESET summary:

- Any pending interrupts are cleared
- I^2C registers are in the default state
- BSI and SDN counter value in the registers are set to four clock cycles or “0000 0100”
- Both on chip regulators are set to 1.8V and disabled
- All SIM1 and SIM2 signals are pulled to GND

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SETTING UP THE SIM INTERFACE

The TXS02326 supports both Class C (1.8V) or Class B (2.95V) SIM cards. In order to support these cards types, the interface on the SIM side needs to be properly setup. After power up, the system should default to SIM1 card. The following sequence outlines a rudimentary sequence of preparing the SIM1 card interface:

- Configure the SIM1 regulator to 1.8V by asserting B1 = 0 in the SIM Interface Control Register (08h). The system by default should start in 1.8V mode.
- Configure the OE signal by asserting B0 = 0 in the Device Control Register (0Eh). The default value essentially disables the OE pin and the device is configured as an auto direction translator.
- The baseband SIM interface is set to a LOW state.
- Disable the SIM1 interface by asserting B2 = 0 and B3 = 0 in the SIM Interface Control Register.
- Disable the SIM2 interface by asserting B6 = 0 and B7 = 0 in the SIM Interface Control Register.
- VSIM1 voltage regulator should now be activated by asserting B0 = 1 in the SIM Interface Control Register.
- Enable the SIM1 interface by asserting B2 = 1 and B3 = 1 in the SIM Interface Control Register.
- The SIM1 interface (VSIM1, SIM1CLK, SIM1I/O) is now active. The TXS02326 relies on the baseband to perform the power up sequencing of the SIM card. If there is lack of communication between the baseband and the SIM card, the SIM1 interface must be powered-down and then powered up again through the regulator by configuring it to 2.95V by asserting B1 = 1 in the SIM Interface Control Register.

SWITCHING BETWEEN SIM CARDS

The following sequence outlines a rudimentary sequence of switching between the SIM1 card and SIM2 card:

- Put the SIM1 card interface into “clock stop” mode then assert B2 = 1 and B3 = 0 in the SIM Interface Control Register (08h). This will latch the state of the SIM1 interface (SIM1CLK, SIM1I/O, SIM1RST).
- There can be two scenarios when switching to SIM2 card:
  - SIM2 may be in the power off mode, B6 = 0 and B7 = 0 in the Status Register (04h). If SIM2 is in power off mode, the SIM/UICC interface will need to be set to the power off state. In this case the baseband will most likely need to go through a power up sequence iteration
  - SIM2 may already be in the “clock stop” mode, B6 = 1 and B7 = 0 in the Status Register (04h). If SIM2 is in “clock stop” mode, the interface between the baseband and the device is set to the clock stop mode levels that correspond to the SIM2 card interface.
- After determining whether the SIM2 card is either in power off mode or clock stop mode, the SIM2 card interface is then activated by asserting B6 = 1 and B7 = 1 in the SIM Interface Control Register (08h) and the negotiation between the baseband and card can continue.
- Switching from SIM2 to SIM1 done in the same manner.

AUTOMATIC SHUTDOWN

Both SIM card interfaces can be configured to automatically shut down upon disconnecting the battery. The shutdown threshold $BSI_{Threshold}$ is configured in B3 of the Device Control Register (0Eh). Two threshold levels are available for this configuration. When the BSI input level exceeds the $BSI_{Threshold}$ level that caused this power-down, both SIM card interfaces will automatically be shut down. If the battery removal interrupt is enabled through B2 of the Device Control Register, then an interrupt will be issued to the baseband on IRQ. This case may happen if the user decides to remove the battery.

There are two scenarios for shutting down each SIM: SIMx is “active”, or in “clock stop” mode. In clock stop mode, when the debounce timer expires, the SIMx signals all go low immediately, then the regulator is disabled one 32KHz cycle later. If SIMx is active, the signals go low and the regulator is disabled in a particular sequence to be described in the next section.

The SIM2 interface can also be configured to automatically shut down via the SDN pin.

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BSI / SDN DEBOUNCE AND AUTOMATIC SHUTDOWN SEQUENCE TIMING

There are two debounce counters: one each for the BSI and SDN inputs. For each counter, when the device is reset or the related input is “false”, the counter is loaded with the value in the associated Debounce Counter register and the debounced signal (i.e. BSI_DEB or SDN_DEB) is subsequently set to a “false” state. When the related input becomes “true”, the counter begins counting down on subsequent CLK rising-edges. (CLK is either the internal or external 32 kHz clock as selected by Clock Source Select)

If the input changes state during the count, the counter is again loaded with the register value. The debounce counter propagates the input signal to the output when the counter expires.

For BSI and BSI_DEB, the “true” state is high. For SDN and SDN_DEB, the “true” state is the state stored in the SDN Detection Level register. Once either count reaches zero, the debounced signal switches to the “true” state on the next CLK rising edge.

If BSI_DEB goes high and Battery Removal Interrupt (bit 2 of the Device Control Register) is 1, an interrupt is generated and appears on IRQ. Also, if BSI_DEB goes high and BSI Detection Control (bit 4 of the Device Control Register) is 0, the Automatic Shutdown sequence begins for both SIM’s.

If SDN_DEB goes “true” and SDN Detection Interrupt (bit 5 of the Device Control Register) is 1, an interrupt is generated and appears on IRQ. Also, if SDN_DEB goes “true” and SDN Detection Control (bit 7 of the Device Control Register) is 0, the Automatic Shutdown sequence begins for SIM2 only, leaving SIM1 unaffected.

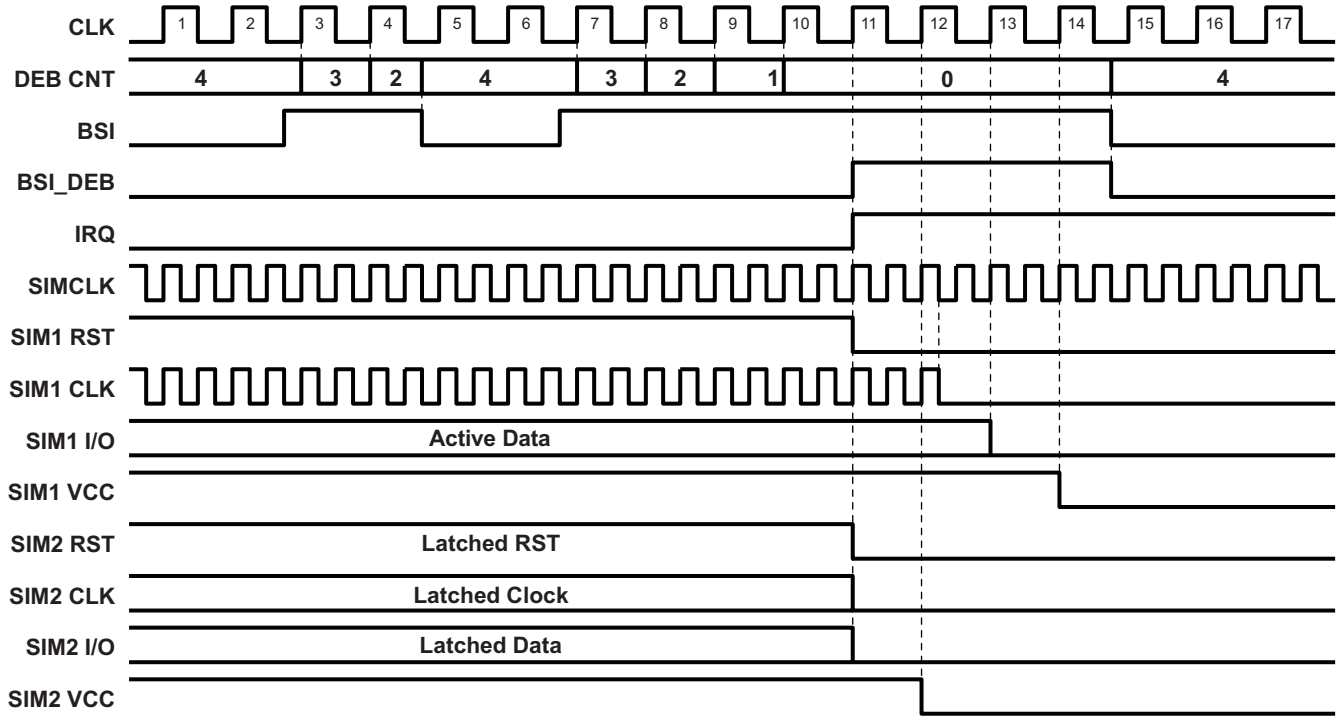


Figure 2. BSI Debounce Timing – SIM1 Active and SIM2 Isolated

Notes:

BSI debounce count value set to 4

SIM1 Active, SIM2 powered but Isolated

BSI Detection Control set to 0

Battery Removal Interrupt set to 1

Once BSI is high for four cycles, BSI_DEB goes high causing automatic shutdown sequence on both SIMs. Since SIM1 is active with SIMCLK running, it follows the staged shutdown sequence. Since SIM2 is powered up but inactive, it follows the instant shutdown sequence.

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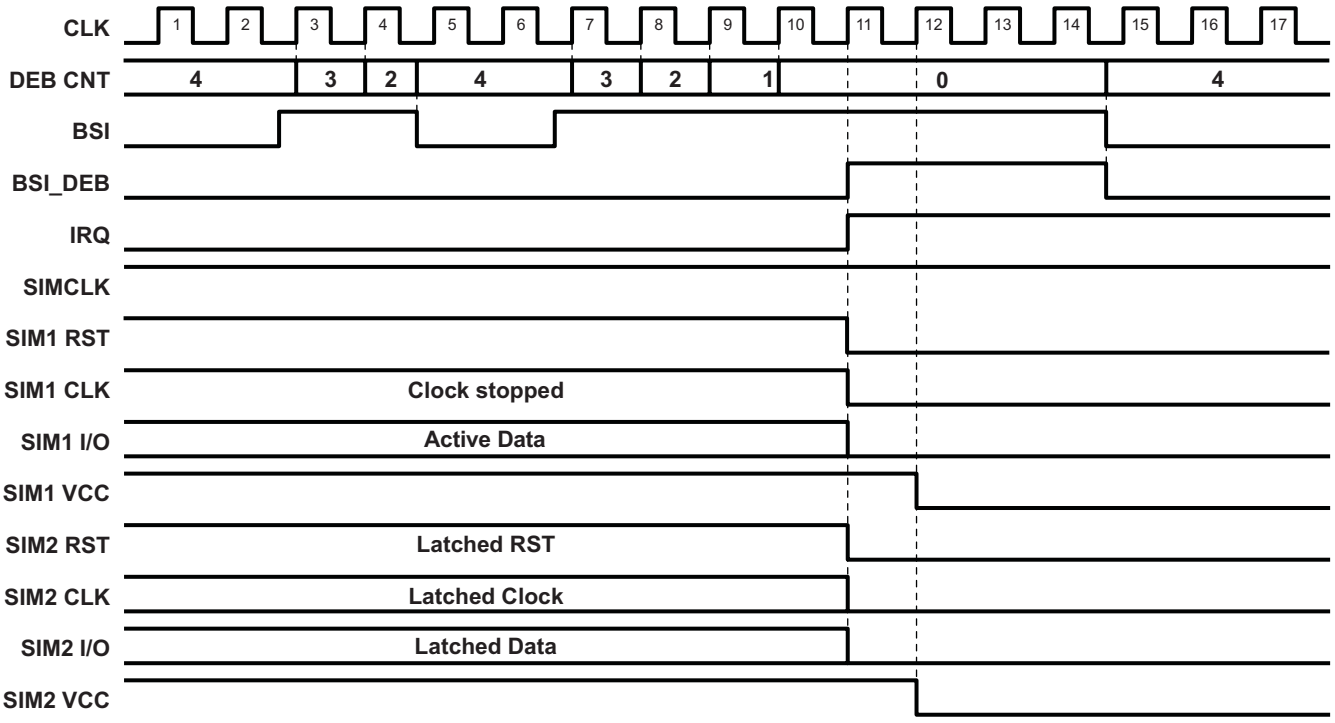


Figure 3. BSI Debounce Timing – SIM1 Clock Stop and SIM2 Isolated

Notes:

BSI debounce counter set to 4

SIM1 Active in Clock Stop Mode

SIM2 powered but Isolated

BSI Detection Control set to 0

Battery Removal Interrupt set to 1

Once BSI is high for four cycles, BSI_DEB goes high causing automatic shutdown sequence on both SIMs. Since SIM1 is active with SIMCLK stopped, it follows the instant shutdown sequence. Since SIM2 is powered up but inactive, it follows the instant shutdown sequence.

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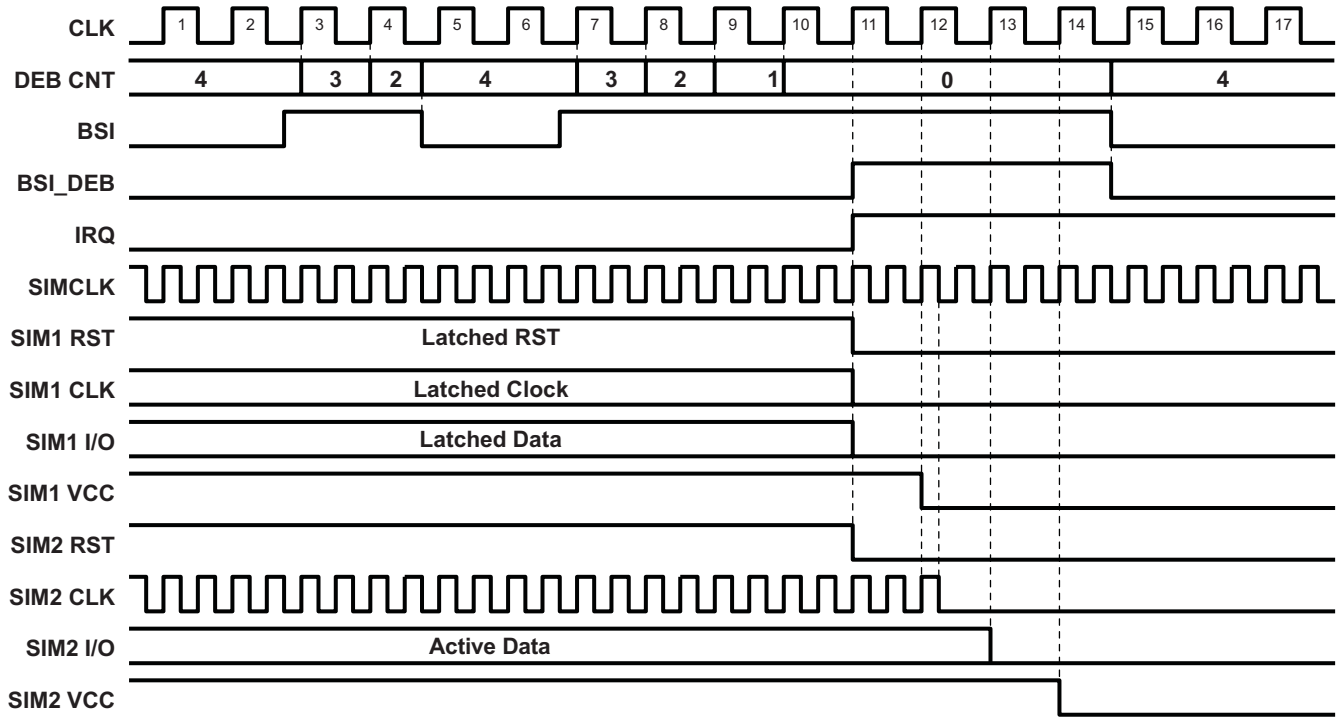


Figure 4. BSI Debounce Timing – SIM1 Isolated, SIM2 Active

Notes:

BSI debounce counter set to 4

SIM2 Active

SIM1 powered but Isolated

BSI Detection Control set to 0

Battery Removal Interrupt set to 1

Once BSI is high for four cycles, BSI_DEB goes high causing automatic shutdown sequence on both SIMs. Since SIM2 is active with SIMCLK running, it follows the staged shutdown sequence. Since SIM1 is powered up but inactive, it follows the instant shutdown sequence.

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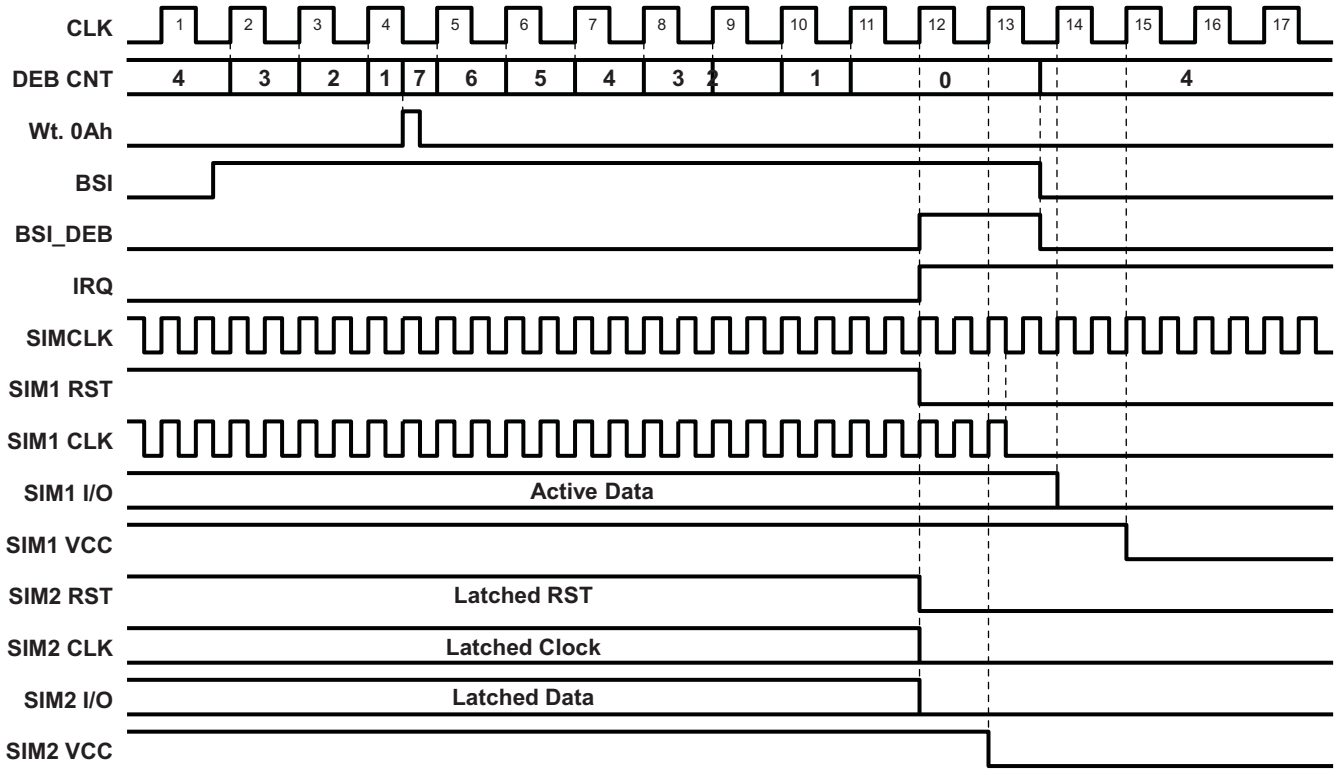


Figure 5. BSI Debounce Timing – Debounce Count Value Write During Debounce

Notes:

BSI debounce count value set to 4, but written to 7 during debounce

SIM1 Active

SIM2 powered but Isolated

BSI Detection Control set to 0

Battery Removal Interrupt set to

BSI_DEB goes high causing automatic shutdown sequence on both SIM's. Since SIM1 follows the staged shutdown sequence. SIM2 follows the instant shutdown sequence. BSI returning low does not interrupt shutdown sequence.

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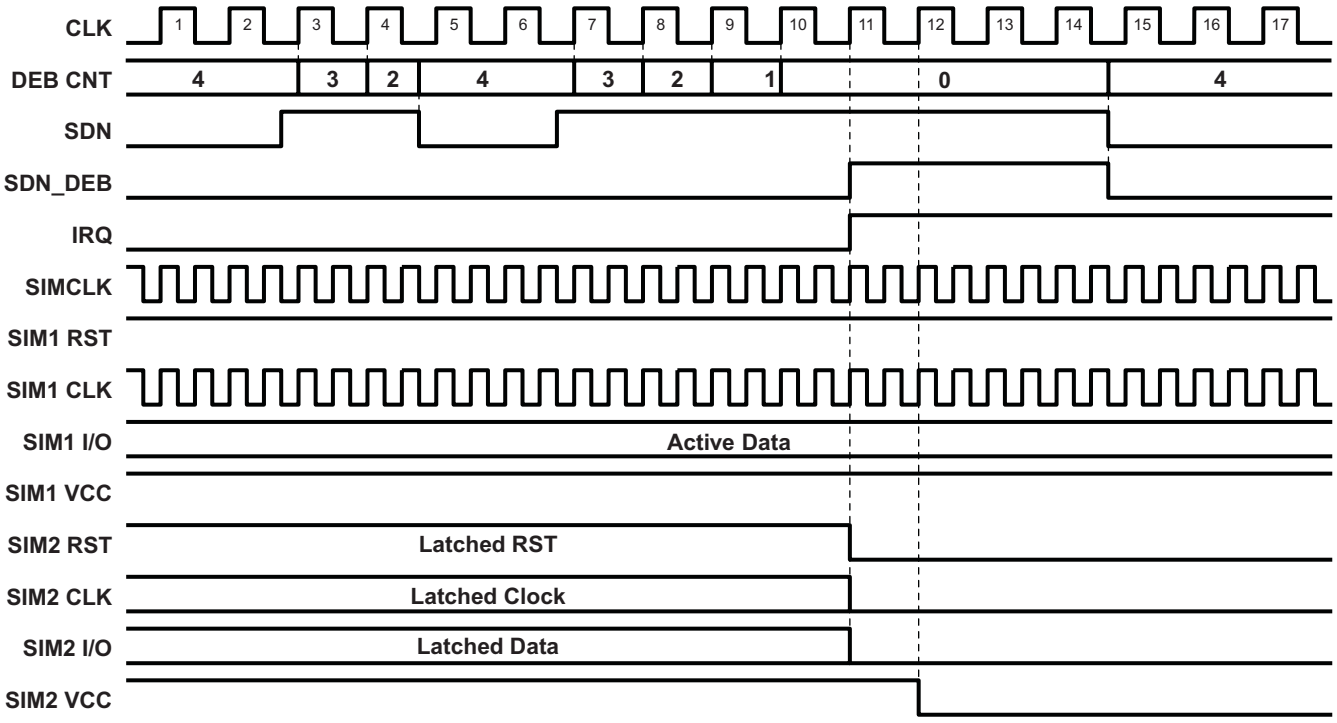


Figure 6. SDN Debounce Timing – SDN Detection Level High

Notes:

SDN debounce count value set to 4

SIM1 Active

SIM2 powered but Isolated

SDN Detection Control set to 0

SDN Detection level set to 1

SDN Detection Interrupt set to 1

Once SDN is high for four cycles, SDN_DEB goes high causing automatic shutdown sequence on SIM2. SIM1 is unaffected. Since SIM2 is powered up but inactive, it follows the instant shutdown sequence.

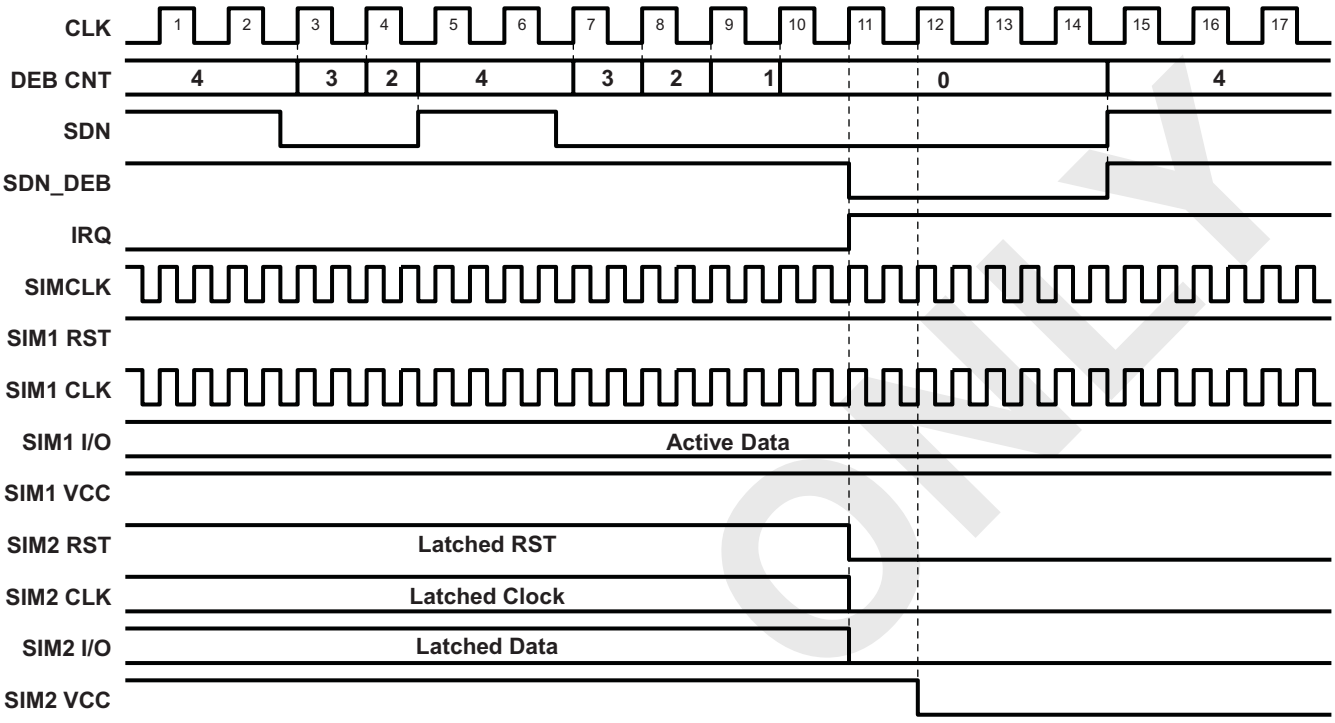


Figure 7. SDN Debounce Timing – SDN Detection Level Low

Notes:

SDN debounce count value set to 4

SIM1 Active

SIM2 powered but Isolated

SDN Detection Control set to 0

SDN Detection level set to 0

SDN Detection Interrupt set to 1

Once SDN is low for four cycles, SDN_DEB goes low causing automatic shutdown sequence on SIM2. SIM1 is unaffected. Since SIM2 is powered up but inactive, it follows the instant shutdown sequence.

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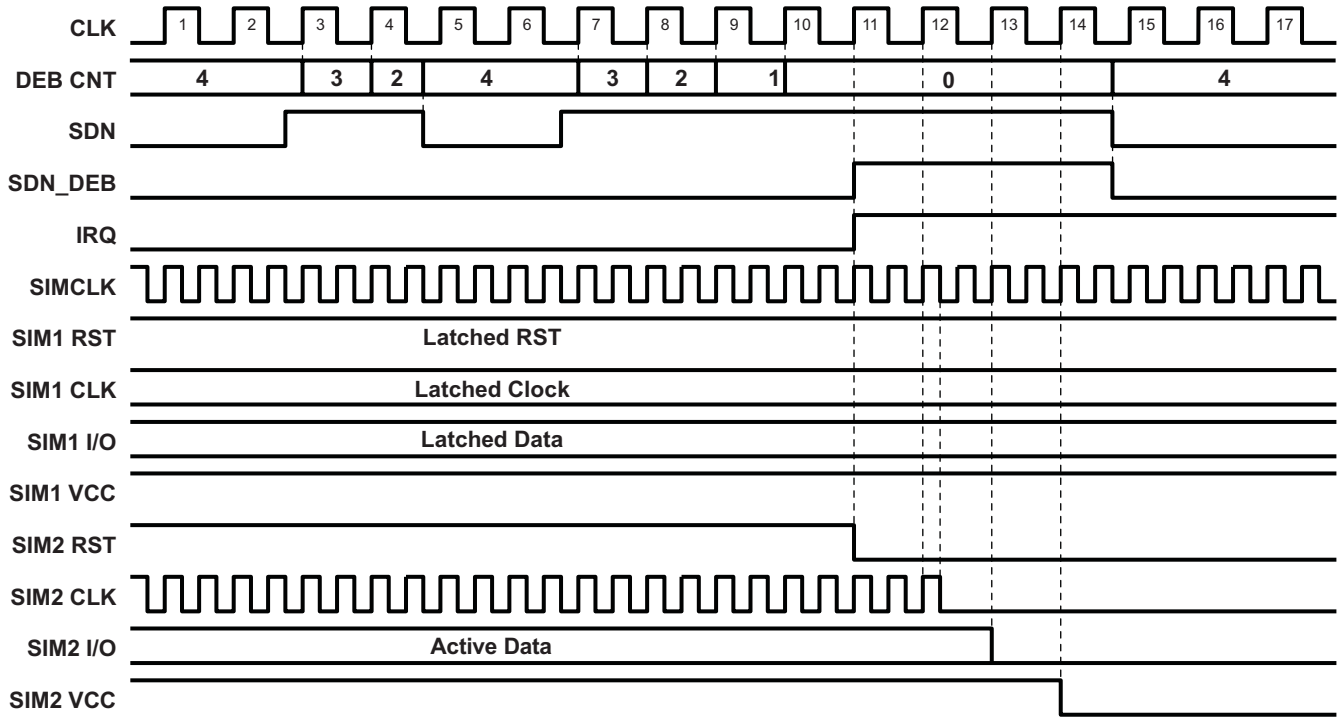


Figure 8. SDN Debounce Timing – SIM1 Isolated and SIM 2 Active

Notes:

SDN debounce count value set to 4

SIM1 powered but Isolated

SIM2 Active

SDN Detection Control set to 0

SDN Detection level set to 1

SDN Detection Interrupt set to 1

SDN_DEB goes high causing automatic shutdown sequence on SIM2. Since SIM2 is active with SIMCLK running, it follows the staged shutdown sequence, SIM1 is unaffected.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

Level Translator(1)

			MIN	MAX	UNIT
$V_{I/O}$	Supply voltage range		–0.3	4.0	V
V_I	Input voltage range	V_I/O-port	–0.5	4.6	V
		VSIMx-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	V_I/O-port	–0.5	4.6	V
		VSIMx-port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state	V_I/O-port	–0.5	4.6	V
		VSIMx-port	–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

LDO(1)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		–0.3	6	V
V_{OUT}	Output voltage range		–0.3	6	V
T_J	Junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–55	150	°C
	ESD rating	Human-Body Model (HBM)		2	kV
		Charged-Device Model (CDM)		1000	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance(1)	RGE package	45	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

Level Translator

		Description	MIN	MAX	UNIT
V_I/O	Supply voltage		1.7	3.3	V
V_{IH}	High-level input voltage	Applies to pins: RESET, SDN, SCL, SDA, IRQ, OE, 32kHz, SIM_RST, SIM_CLK, SIM_I/O	V_I/O × 0.7	1.9	V
V_{IL}	Low-level input voltage		0	V_I/O × 0.3	V
Δt/Δv	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS
Level Translator

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_I/O	VSIM1	VSIM2	MIN	TYP(1)	MAX	UNIT
V_{OH}	SIM1_RST	I_{OH} = –100 µA Push-Pull	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)	VSIM1 × 0.8			V
	SIM1_CLK					VSIM1 × 0.8			
	SIM1_I/O	I_{OH} = –10 µA Open-Drain				VSIM1 × 0.8			
		I_{OH} = –100 µA Push-Pull							
	SIM2_RST	I_{OH} = –100 µA Push-Pull				VSIM2 × 0.8			
	SIM2_CLK					VSIM2 × 0.8			
	SIM2_I/O	I_{OH} = –10 µA Open-Drain				VSIM2 × 0.8			
		I_{OH} = –100 µA Push-Pull							
	SIM_I/O	I_{OH} = –10 µA Open-Drain				V_I/O × 0.8			
		I_{OH} = –100 µA Push-Pull							
V_{OL}	SIM1_RST	I_{OL} = 1 mA Push-Pull	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			VSIM1 × 0.2	V
	SIM1_CLK	I_{OL} = 1 mA Push-Pull						VSIM1 × 0.2	
	SIM1_I/O	I_{OL} = 1 mA Open-Drain						0.3	
		I_{OL} = 1 mA Push-Pull							
	SIM2_RST	I_{OL} = 1 mA Push-Pull						VSIM2 × 0.2	
	SIM2_CLK	I_{OL} = 1 mA Push-Pull						VSIM2 × 0.2	
	SIM2_I/O	I_{OL} = 1 mA Open-Drain						0.3	
		I_{OL} = 1 mA Push-Pull							
	SIM_I/O	I_{OL} = 1 mA Open-Drain						0.3	
		I_{OL} = 1 mA Push-Pull							
I_I	Control inputs	V_I = OE	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			±1	µA
$I_{CC\ I/O}$		V_I = V_{CCI} I_O = 0	1.7 V to 3.3 V	1.8 V / 2.95 V (Supplied by LDO)	1.8 V / 2.95 V (Supplied by LDO)			±5	µA
C_{io}	SIM_I/O port						7		pF
	SIMx port						4		
C_i	Control inputs	V_I = V_I/O or GND					3		pF
	Clock input								

(1) All typical values are at T_A = 25°C.

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ELECTRICAL CHARACTERISTICS
LDO (Control Input Logic = High)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
VBAT	Input voltage			2.3		5.5	V
V_{OUT}	Output voltage	Class-B Mode		2.85	2.95	3.05	V
		Class-C Mode		1.7	1.8	1.9	
V_{DO}	Dropout voltage	I_{OUT} = 50 mA				100	mV
I_{GND}	Ground-pin current	I_{OUT} = 0 mA				35	µA
		I_{OUT} = 50 mA				150	
I_{SHDN}	Shutdown current (I_{GND})	V_{ENx} ≤ 0.4 V, (VSIMx + V_{DO}) ≤ VBAT ≤ 5.5 V, T_J = 85°C				3	µA
$I_{OUT(SC)}$	Short-circuit current	R_L = 0 Ω				400	mA
C_{OUT}	Output Capacitor				1		µF
PSRR	Power-supply rejection ratio	VBAT = 3.25 V, VSIMx = 1.8 V or 3 V, C_{OUT} = 1 µF, I_{OUT} = 50 mA	f = 1 kHz	50			dB
			f = 10 kHz	40			
T_{STR}	Start-up time	VSIMx = 1.8 V or 3 V, I_{OUT} = 10 mA, C_{OUT} = 1 µF				50	µS
T_J	Operating junction temperature			–40		85	°C

(1) All typical values are at T_A = 25°C.

GENERAL ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BSI_{Threshold}$	Comparator Threshold	BSI detection level “1”	1.6		1.7	V
		BSI detection level “0”	1.1		1.3	
Hyst	Internal hysteresis of comparator			±50		mV
CLK_{Int}	Internal System Clock		–20%	32	+20%	KHz
R_{SIMPU}	SIM I/O pull-up		18	20	22.6	kΩ
R_{SIMxPU}	SIMx I/O pull-up	Class B	6	7.5	9	kΩ
		Class C	3.8	4.5	5.2	
R_{SIMPD}	SIMx I/O pull-down	Active pull-downs are connected to the VSIM1/2 regulator output to the SIM1/2 CLK, SIM1/2 RST, SIM1/2 I/O when the respective regulator is disabled			2	kΩ

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SWITCHING CHARACTERISTICS
VSIMx = 1.8 V or 2.95 V Supplied by Internal LDO, VBAT = 2.3V to 5.5V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_I/O = 1.7 V to 3.3 V		UNIT
			MIN	MAX	
t_{rA} Baseband side to SIM side	SIM_I/O	Open Drain		210	ns
	SIM_I/O	Push Pull		8.6	ns
	SIM_RST	Push Pull		4.3	ns
	SIM_CLK	Push Pull		4	ns
t_{rA} Baseband side to SIM side	SIMx_I/O	Open Drain		16	ns
	SIMx_I/O	Push Pull		6.5	ns
	SIM_RST	Push Pull		4	ns
	SIMx_CLK	Push Pull		5	ns
t_{rB} SIM side to Baseband side	SIMx_I/O	Open Drain		210	ns
	SIMx_I/O	Push Pull		10	ns
t_{rB} SIM side to Baseband side	SIMx_I/O	Open Drain		6	ns
	SIMx_I/O	Push Pull		8	ns
f_{max}	SIMx_CLK	Push Pull		5	MHz
t_{PLH}	SIMCLK to SIMx_CLK	Push Pull		8	ns
	SIMRST to SIMx_RST	Push Pull		8	ns
	SIMIO to SIMx_IO	Open Drain		260	ns
	SIMIO to SIMx_IO	Push Pull		10	ns
	SIMx_IO to SIMIO	Open Drain		260	ns
	SIMx_IO to SIMIO	Push Pull		10.5	ns
t_{PLH}	SIMCLK to SIMx_CLK	Push Pull		7	ns
	SIMRST to SIMx_RST	Push Pull		7	ns
	SIMIO to SIMx_IO	Open Drain		23	ns
	SIMIO to SIMx_IO	Push Pull		8	ns
	SIMx_IO to SIMIO	Open Drain		23	ns
	SIMx_IO to SIMIO	Push Pull		10	ns

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OPERATING CHARACTERISTICS

T_A = 25°C, V_{SIMx} = 1.8 V for Class C, V_{SIMx} = 2.95 V for Class B

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} (1)	Class B	C_L = 0, f = 5 MHz, $t_r = t_f$ = 1 ns	11	pF
	Class C		9.5	

(1) Power dissipation capacitance per transceiver

APPLICATION INFORMATION

The LDO's included on the TXS02326 achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom (V_{BAT} – $V_{SIM1/2}$). The TXS02326 provides fixed regulation at 1.8V or 2.95V. Low noise, enable (through I^2C control), low ground pin current make it ideal for portable applications. The device offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to +85°C.

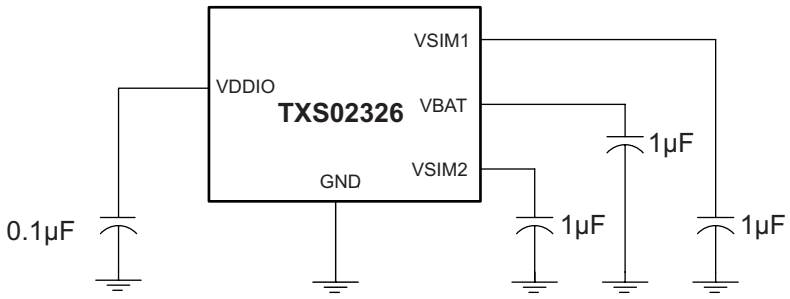


Figure 9. Typical Application circuit for TXS02326

Input and Output Capacitor Requirements

It is good analog design practice to connect a 1.0 µF low equivalent series resistance (ESR) capacitor across the input supply (VBAT) near the regulator. Also, a 0.1uF is required for the logic core supply (VDDIO).

This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. The LDO's are designed to be stable with standard ceramic capacitors of values 1.0 µF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be < 1.0 Ω.

Output Noise

In most LDO's, the bandgap is the dominant noise source. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TXS02326 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TXS02326 has a built-in body diode that conducts current when the voltage at $V_{SIM1/2}$ exceeds the voltage at V_{BAT}. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Dropout Voltage

The TXS02326 uses a PMOS pass transistor to achieve low dropout. When (V_{BAT} – $V_{SIM1/2}$) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

Startup

The TXS02326 uses a quick-start circuit which allows the combination of very low output noise and fast start-up times. Note that for fastest startup, V_{BATT} should be applied first, and then enabled by asserting the I^2C register.

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Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

Minimum Load

The TXS02326 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TXS02326 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +85°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +85°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TXS02326 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TXS02326 into thermal shutdown will degrade device reliability.

TYPICAL CHARACTERISTICS

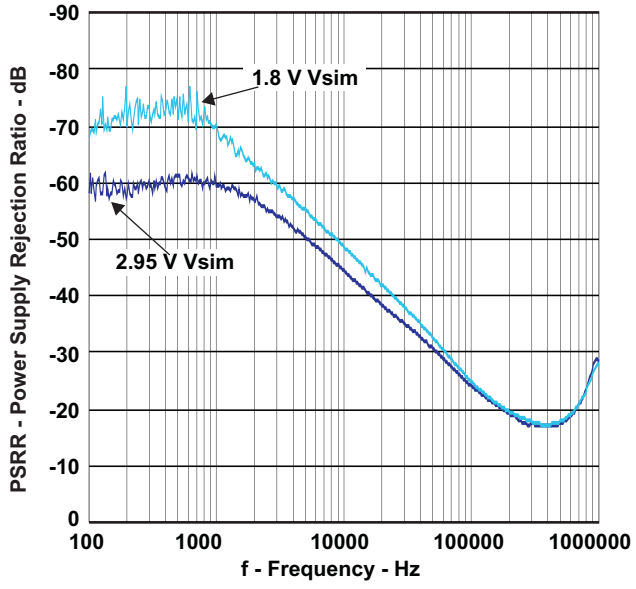


Figure 10. PSRR

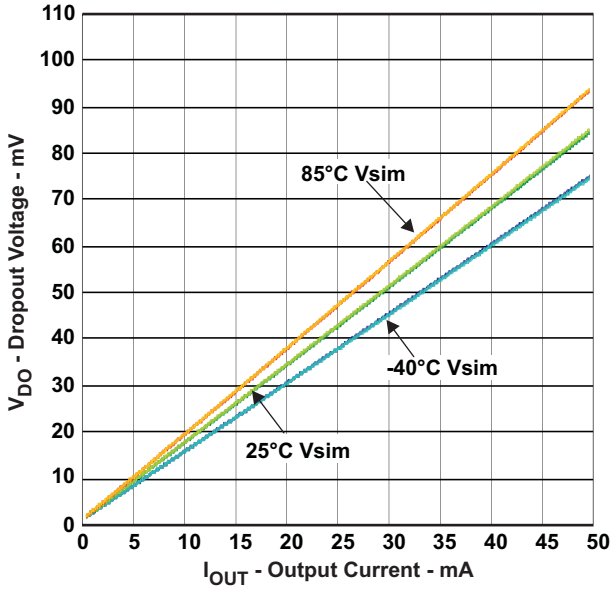


Figure 11. Dropout Voltage vs Output Current

TYPICAL CHARACTERISTICS (continued)

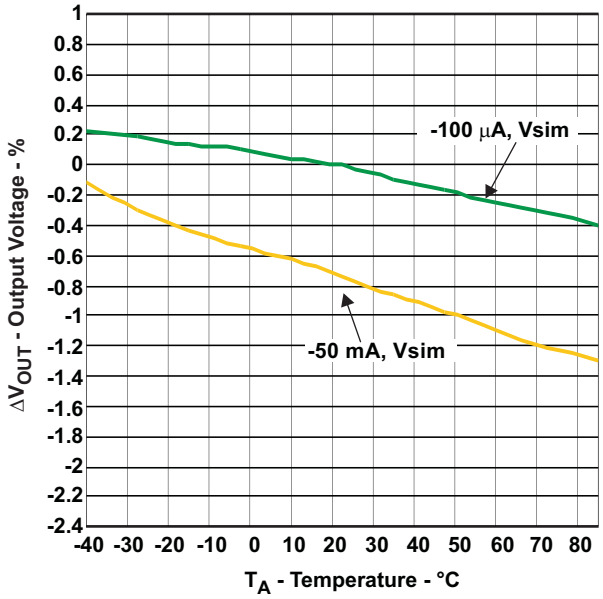


Figure 12. Output Voltage vs Temperature, Class-B/C

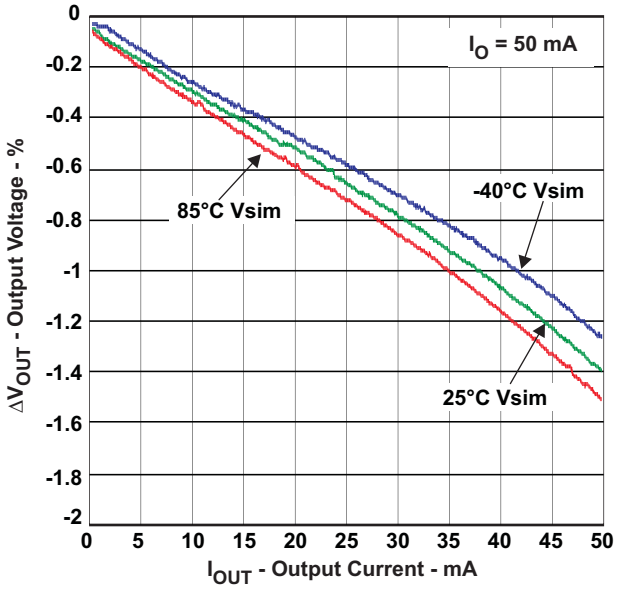


Figure 13. Load Regulation, Iout = 50 mA, Class-C

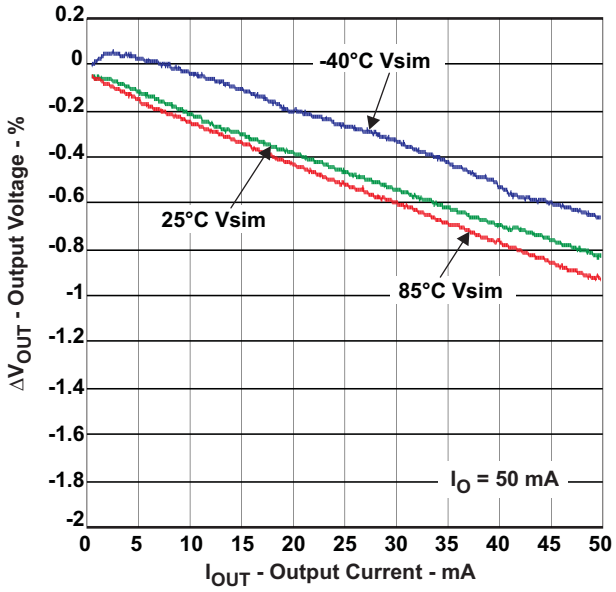


Figure 14. Load Regulation, Iout = 50 mA, Class-B

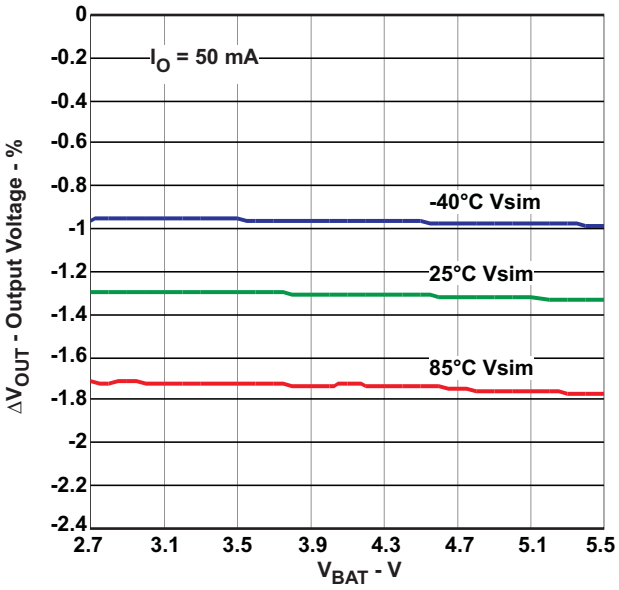


Figure 15. Line Regulation, Iout = 50 mA, Class-C

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TYPICAL CHARACTERISTICS (continued)

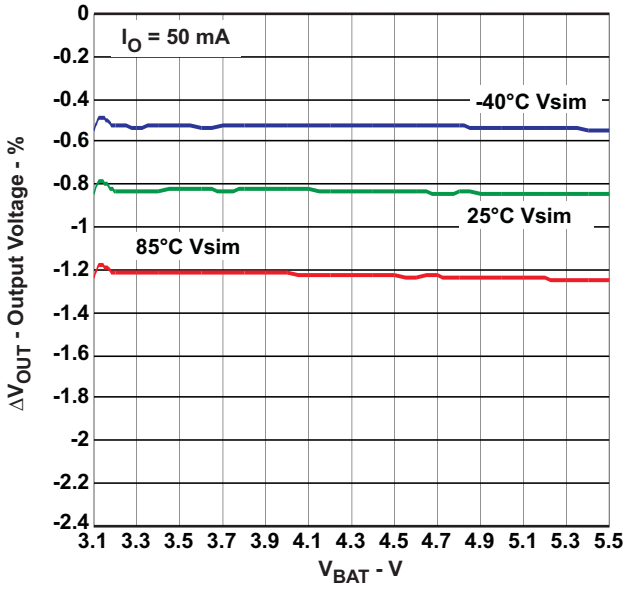


Figure 16. Line Regulation, Iout = 50 mA, Class-B

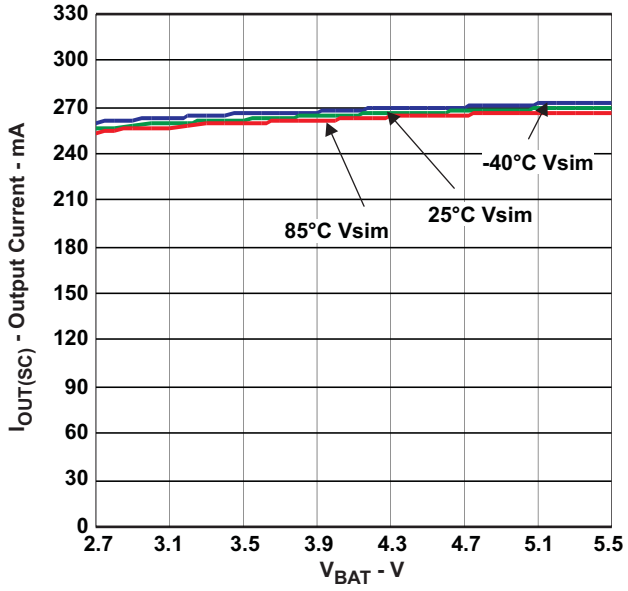


Figure 17. Current Limit vs Input Voltage, Class-B/C

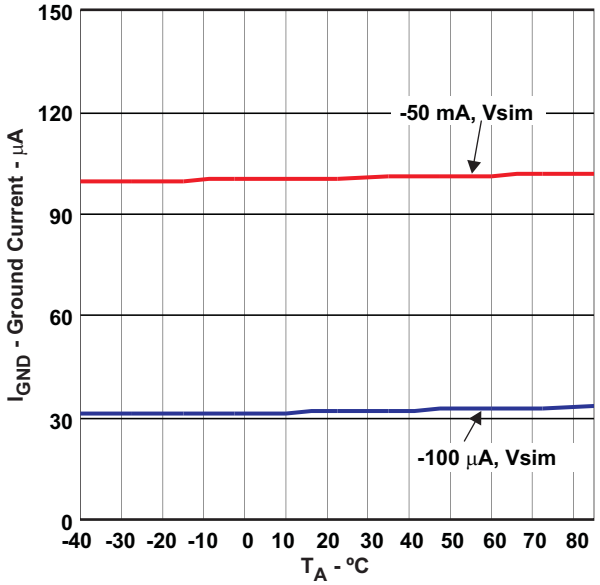


Figure 18. Ground Current vs Temperature, Class-C

REVISION HISTORY

Changes from Revision A (November 2010) to Revision B	Page
• Added TYPICAL CHARACTERISTICS Section	25

Changes from Revision B (November 2010) to Revision C	Page
• Added hardware and software contol registers, previously undefined values.	4

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS02326MRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		YJ326	Samples
TXS02326RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		YJ326	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

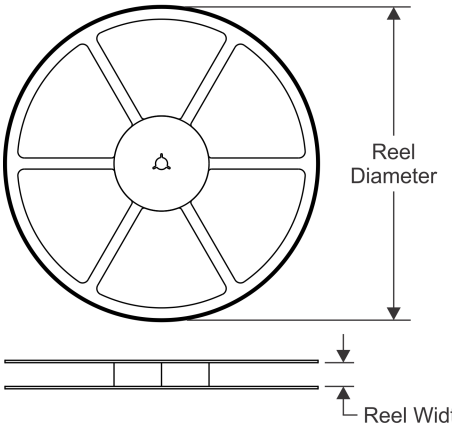
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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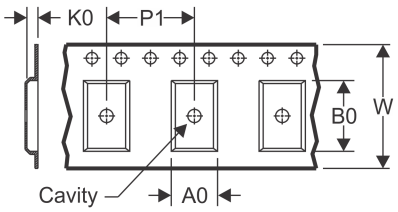
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

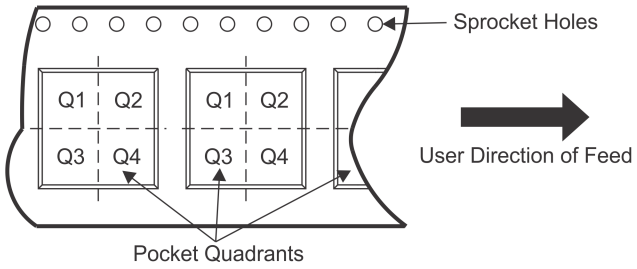


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

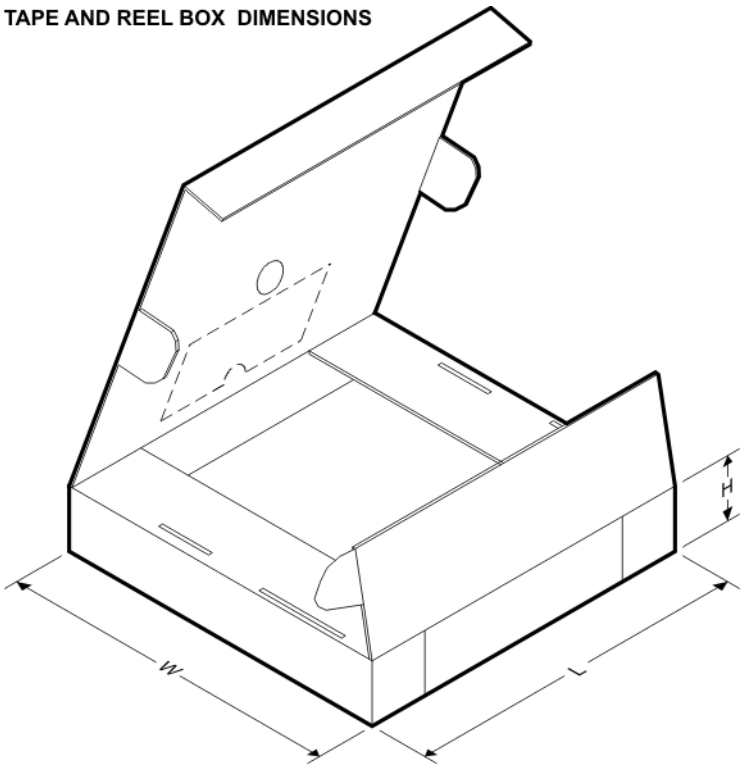
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS02326MRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



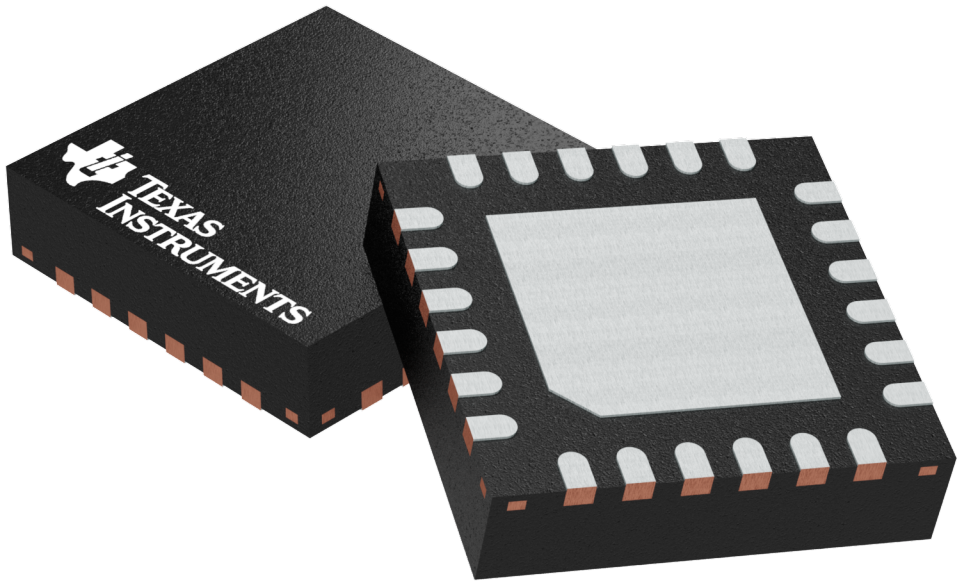
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS02326MRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

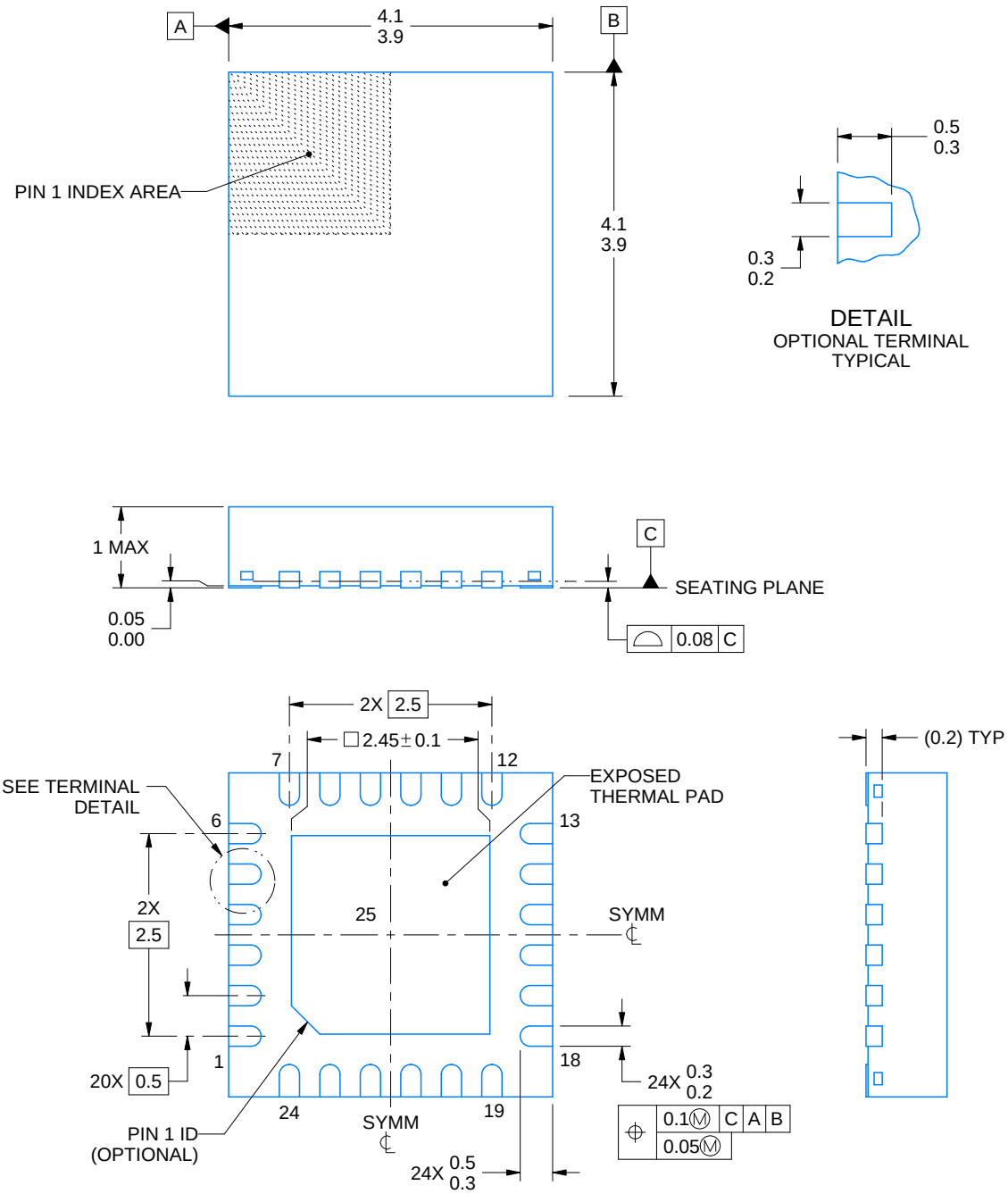
4204104/H

PACKAGE OUTLINE

RGE0024B

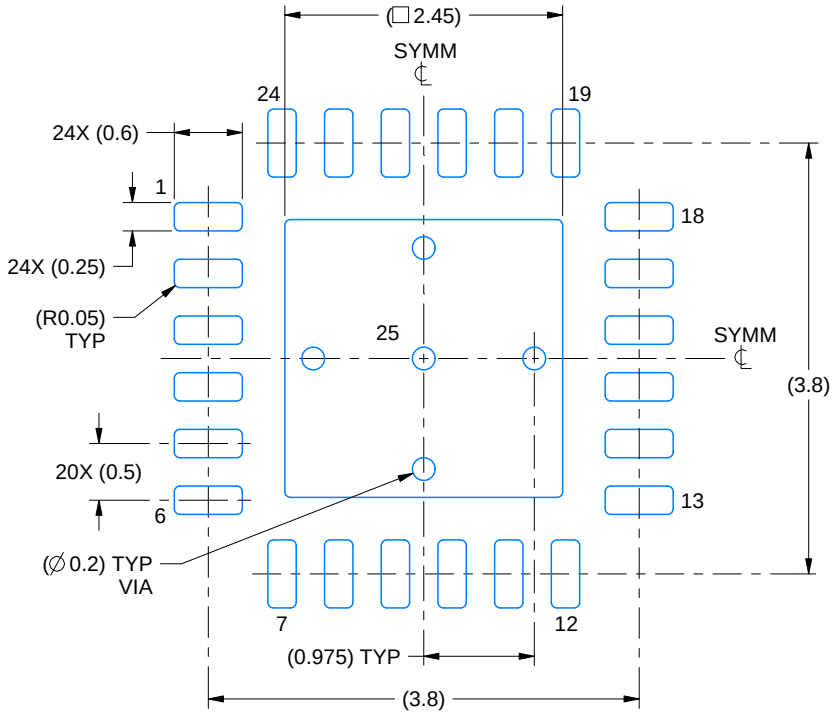
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

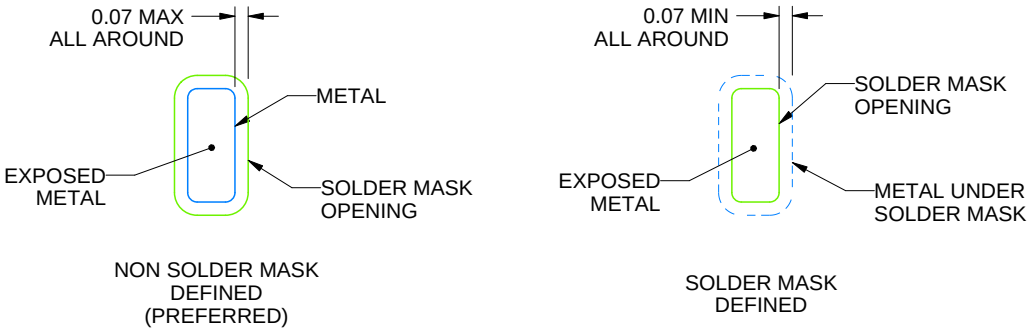


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

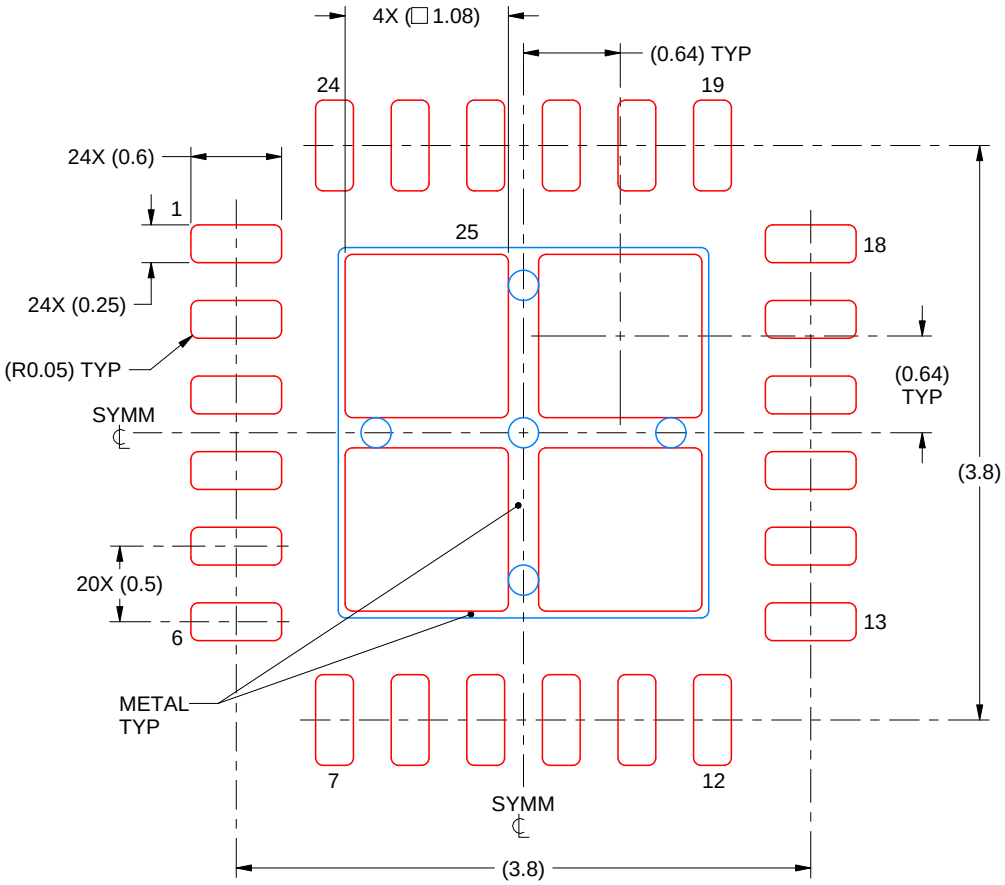


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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